an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,

wherein said at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, and

wherein at least two adjacent dummy lead wires provided on one side of said insulating film have tip portions connected to each other on the semiconductor element.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 28 and 29 are pending in the present application. Claim 28 has been amended by the present amendment.

In the outstanding Office Action, the drawings were objected to; Claim 28 was objected under 35 U.S.C. § 112, first paragraph; Claim 28 was rejected under 35 U.S.C. § 103(a) as unpatentable over Oshino et al in view of Sugimoto et al; and Claim 29 was rejected under 35 U.S.C. § 103(a) as unpatentable over Oshino et al in view of Candelore.

In response to the objection to the drawings, Claim 28 has been amended to recite features shown in the filed figures. Accordingly, it is respectfully requested this objection be

withdrawn.

In response to the rejection of Claim 28 under 35 U.S.C. § 112, first paragraph, Claim 28 has been amended to cancel a feature indicated in the outstanding Office Action at page 3, item 5. In addition, Claim 28 has been amended to more clearly recite a feature that finds support in Figure 4A, reference 33'. Accordingly, it is respectfully requested this rejection be withdrawn.

Claim 28 was rejected under 35 U.S.C. § 103(a) as unpatentable over Oshino et al in view of Sugimoto et al. This rejection is respectfully traversed.

Amended Claim 28 is directed to a semiconductor memory device having a semiconductor element, a plurality of lead wires, and at least a single dummy lead wire. Further, the at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires from the plurality of lead wires such that a length of the space is at least twice a minimum pitch between the adjacent lead wires. In addition, at least two adjacent dummy lead wires are provided on one side of an insulating film having an opening to accommodate the semiconductor device and the at least two adjacent dummy lead wires have tip portions connected to each other on the semiconductor element.

In a non-limiting example, Figure 2A shows the semiconductor element 11, the insulating film 12, the plurality of lead wires 13, and the at least a single dummy lead wire 13'. Further, Figure 4A show two adjacent dummy lead wires 33' provided on one side of the insulating film 32 and having the tip portions connected to each other on the semiconductor element 31.

Oshino et al shows in Figures 1 and 2 a semiconductor memory device having a semiconductor element 3, a plurality of lead wires 5, and at least a single dummy lead wire 5B. The outstanding Office Action asserts at page 5, lines 7-10, that Oshino et al show a

single dummy lead wire 5B (right) arranged in a space defined by two adjacent lead wires of the plurality of lead wires 5 such that a length of the space is at least twice a minimum pitch between adjacent lead wires. However, it is respectfully submitted that Oshino et al do not teach or suggest at least a single dummy lead wire 5B (right) arranged in the space defined by two adjacent lead wires 5 such that the length of the space is at least twice a minimal pitch between adjacent lead wires. Oshino et al show in Figure 1 a dummy lead wire 5B placed next to a lead wire 5A and the lead wire 5A lacks another lead wire placed next to the lead wire 5A to define a space between these two lead wires. In addition, Oshino et al do not teach of suggest tip portions of the at least two adjacent dummy lead wires connected to each other on the semiconductor element.

The outstanding Office Action asserts Sugimoto et al for teaching adjacent dummy lead wires connected to each other. Sugimoto et al show in Figure 1 adjacent dummy lead wires 7 connected to each other but not at tip portions on a semiconductor element, as recited in Claim 28. Therefore, Sugimoto et al do not teach or suggest at least two adjacent dummy lead wires having tip portions connected to each other on the semiconductor element.

Accordingly, it is respectfully submitted independent Claim 28 patentably distinguishes over the applied art.

Claim 29 was rejected under 35 U.S.C. § 103(a) as unpatentable over Oshino et al in view of Candelore. This rejection is respectfully traversed.

Claim 29 recites similar features to Claim 28, which has been discussed above. More specifically, Claim 29 recites that at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires such that a length of a space formed by the two adjacent lead wires is at least twice a minimum pitch between the adjacent lead wires. As discussed above, Oshino et al do not teach or suggest this feature.

Candelore discloses in Figure 4 a semiconductor device that is stabilized with bond wires 421, 423, and 425. However, Candelore does not teach or suggest a single dummy lead wire arranged in a space defined by two adjacent lead wires such that a length of the space is at least twice a minimum pitch between the adjacent lead wires.

Accordingly, it is respectfully submitted independent Claim 29 is also allowable.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

Please amend Claim 28 as follows:

--28. (Amended) A semiconductor memory device comprising:

a semiconductor element;

a plurality of lead wires connected to a plurality of connecting electrodes formed on said semiconductor element;

at least a single dummy lead wire that is not electrically connected to said semiconductor element and does not include an outer lead portion for electrically connecting said semiconductor element to an external circuit of said semiconductor element;

an insulating film having an opening portion configured to accommodate said semiconductor element and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor element and said at least the single dummy lead wire; and

a resin molding configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,

wherein said at least a single dummy lead wire is arranged in a space defined by two adjacent lead wires of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, and

[wherein the tip portion of said at least the single dummy lead wire covered with said

resin molding is positioned between a peripheral portion of said opening portion and a peripheral portion of the semiconductor element arranged within the opening portion, and]

wherein at least two adjacent dummy lead wires provided on one side of said insulating film have [are arranged on said semiconductor device and] tip portions [of the at least two adjacent dummy lead wires, which have no lead wires therebetween, are] connected to each other on the semiconductor element.--